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? Title: **FR2752466A1: DISPOSITIF PROCESSEUR INTEGRE DE SIGNAUX NUMERIQUES**

? Derwent Title: Integrated digital signal processor for parallel asymmetric processing of video and audio multi-media - has general purpose processor and vector processor operating in parallel and sharing access to common memory cache
[Derwent Record]

? Country: **FR** France
? Kind: **A1** Application, First Publication ¹ (See also: FR2752466B1)

? Inventor: **LE TRONG NGUYEN;**

? Assignee: **SAMSUNG ELECTRONICS CO LTD** Republic of Korea
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? Published / Filed: **1998-02-20** / 1997-08-18

? Application Number: **FR1997000010434**

? IPC Code: Advanced: **G06F 9/38**; **G06F 15/78**;
Core: **G06F 15/76**; more...
IPC-7: **G06F 9/06**; **G06F 15/76**;

? ECLA Code: **G06F9/38S6C**; G06F9/38S4; G06F15/78V2;

? Priority Number: 1996-08-19 **US1996000697102**

? INPADOC Legal Status: None   **Get Now:** Family Legal Status Report

? Family:

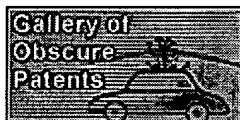| PDF	Publication	Pub. Date	Filed	Title
	US6425054B1	2002-07-23		
▨	US6425054	2002-07-23	2000-10-10	Multiprocessor operation in a multimedia processor
☑	JP10091596A2	1998-04-10	1997-08-19	MULTIPROCESSOR DRIVING DEVICE MULTIMEDIA SIGNAL PROCESSOR
☑	FR2752466B1	2005-01-07	1997-08-18	DISPOSITIF PROCESSEUR INTEGRE I SIGNAUX NUMERIQUES
☑	FR2752466A1	1998-02-20	1997-08-18	DISPOSITIF PROCESSEUR INTEGRE I SIGNAUX NUMERIQUES
☑	DE19735981A1	1998-03-26	1997-08-19	Mehrprozessorbetrieb in einem Multimed Signalprozessor
☑	CN1175037A	1998-03-04	1997-08-07	MULTI-PROCESSOR OPERATOR IN M MEDIA SIGNAL PROCESSOR
☑	CN1129078C	2003-11-26	1997-08-07	Integrated digital signal processor

8 family members shown above

Forward References:

PDF	Patent	Pub.Date	Inventor	Assignee	Title
	US6968452	2005-11-22	Vorbach; Martin	PACT XPP Technologies AG	Method of self-synchroniz configurable elements of programmable unit

Other Abstract Info: None

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？Title: **US6425054: Multiprocessor operation in a multimedia signal proces**

？Derwent Title: Integrated digital signal processor for parallel asymmetric processing of video and audio multi-media - has general purpose processor and vector processor operating in parallel and sharing access to common memory cache [Derwent Record]

？Country: **US** United States of America

？Inventor: **Nguyen, Le Trong**; Monte Sereno, CA

？Assignee: **Samsung Electronics Co., Ltd.**, Kyungki-do, Republic of Korea
other patents from SAMSUNG ELECTRONICS CO., LTD. (491065) (approx. 12,932)
♀Corporate Tree data: Samsung Electronics Co Ltd (SAMSELEC); News, Profiles, Stocks and More about this company
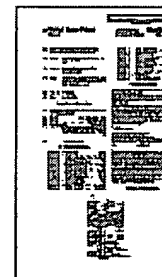
？Published / Filed: **2002-07-23 / 2000-10-10**

？Application Number: **US2000000685982**

？IPC Code: Advanced: **G06F 9/38**; **G06F 15/78**;
Core: **G06F 15/76**; more...
IPC-7: **G06F 12/08**; G06F 13/00;

？ECLA Code: **G06F9/38S4**; G06F9/38S6C; G06F15/78V2;

？U.S. Class: **711/117**; 711/118;

？Field of Search: 711/117,118,130,140,147,149 712/001-9,24,29,32-35 345/501-506,514-522 710/131,132

？Priority Number: 2000-10-10 **US2000000685982**
1996-08-19 **US1996000697102**

？Abstract: To achieve high performance at low cost, an integrated digital signal processor uses an architecture which includes both a general purpose processor and a vector processor. The integrated digital signal processor also includes a cache subsystem, a first bus and a second bus. The cache subsystem provides caching and data routing for the processors and buses. Multiple simultaneous communication paths can be used in the cache subsystem for the processors and buses. Furthermore, simultaneous reads and writes are supported to a cache memory in the cache subsystem.

？Attorney, Agent or Firm: **Skjerven Morrill LLP** ;

？Primary / Asst. Examiners: **Yoo, Do Hyun**; Encarnacion, Yamir

？INPADOC None   Get Now: Family Legal Status Report

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